Claims

1. A signal transmitting apparatus for sending and receiving a plurality of digital input signals input to said signal transmitting apparatus through a single signal line, said signal transmitting apparatus comprising:

a sending part for converting each width of the plurality of digital input signals into a voltage in accordance with a predetermined weight, generating a send signal by adding voltages converted from the plurality of digital input signals, and outputting the send signal; and

a receiving part for receiving the send signal from the sending part, comparing the send signal with a plurality of predetermined voltages, generating each of the digital input signals, and outputting said each of the digital input signals.

2. The signal transmitting apparatus as claimed in claim 1, wherein said sending part includes input resistances, of which number is a same number as the digital signals, and an inversion amplifying circuit formed by an operational amplifier, wherein a resistance value of each of the input resistances connecting to the inverting input terminals of the operational amplifier is set to correspond to a weight of said each width of the digital input signals.

3. The signal transmitting apparatus as claimed in claim 2, wherein a combined resistance value in a case of connecting the input resistances in series is approximately equal to a feedback resistance value of the operational amplifier.

4. The signal transmitting apparatus as claimed in claim 2, wherein the resistance value of each of the input resistances is weighted by a multiple of two.

5. The signal transmitting apparatus as claimed in claim 2, wherein a voltage of a non-inverting input terminal of the operational amplifier is set to be approximately half a power voltage.

6. The signal transmitting apparatus as claimed in claim 1, wherein said receiving part includes:

a reference voltage generating circuit for generating a plurality of predetermined reference voltages;

a voltage comparing circuit for comparing each of the plurality of predetermined reference values with a signal received from said sending part, and outputting a signal showing each comparison result; and

a logic circuit for synthesizing each digital input signal from each output signal of said voltage comparing circuit in accordance with a predetermined method,

wherein said reference voltage generating circuit generates each of the plurality of reference voltages, of which number is resulted from multiplying a number of the digital input signals by two and subtracting one, and outputs said each of the plurality of reference voltages.

7. The signal transmitting apparatus as claimed in claim 6, wherein in a case of two digital input signals, in response to an output signal from said voltage comparing circuit for detecting one digital input signal which weight is greater than another digital input signal, said logic circuit cancels one of the output signals from the voltage comparing circuit for detecting another digital input signal.

8. The signal transmitting apparatus as claimed in claim 1, wherein said sending part adds the voltages being converted while a digital input signal having a greatest weight in the digital input signals is a predetermined signal level.

9. The signal transmitting apparatus as claimed in claim 8, wherein said sending part includes:

a plurality of switching circuits each being controlled by each respective digital input signal; and

a plurality of load resistances each being connected to each switching circuit in series,

wherein one load resistance connected to one switching circuit, which is controlled by one digital input signal having a greatest weight, is connected between a predetermined voltage and the relative switching circuit, and a series circuit for other switching circuits and relative resistances is connected to the one switching circuit, which is controlled by the one digital input signal having the greatest weight, in parallel.

10. The signal transmitting apparatus as claimed in claim 9, wherein the one load resistance connected to the one switching circuit, which is controlled by the one digital input signal having the greatest weight, is set to be the same resistance value as a combined resistance value when the other load resistances are connected in parallel.

11. The signal transmitting apparatus as claimed in claim 1, wherein said receiving part includes:

a reference voltage generating circuit for generating and outputting each of a plurality of predetermined reference voltages;

a voltage comparing circuit for comparing each of the plurality of predetermined reference voltages and a signal received from said sending part, and outputting a signal showing each comparison result; and

a logic circuit for synthesizing each of the digital

input signals from each output signal of said voltage comparing circuit in accordance with a predetermined method.

12. The signal transmitting apparatus as claimed in claim 11, wherein in a case of two digital input signals, said logic circuit output said each output signal as each of the digital signals received from the voltage comparing circuit.

13. A power supplying system for supplying a power from a plurality of power supplying devices to each of a plurality of loads, said power supplying system comprising:

a first power supplying device including a first power supplying part for supplying a power to at least one of the plurality of loads, a controlling part for conducting an operation control of the first power supplying part, and a first communicating part for sending and receiving a signal to and from the controlling part; and

at least one second power supplying device including a second power supplying part for supplying a power to at least one of the plurality of loads, and a second communicating part for sending and receiving a signal to and from the second power supplying part,

wherein the first communicating part and the second communicating part send and receive signals each other, and the controlling part conducts the operation control of the second power

supplying part through the first communicating part and the second communicating part.

14. The power supplying system for supplying a power from a plurality of the power supplying devices to a plurality of loads, said power supplying system comprising:

a first power supplying device including a first power supplying part for supplying a power to at least one of the plurality of loads, and a first power supplying device including a first communicating part for sending and receiving a signal with an external device;

at least one second power supplying device including a second power supplying part for supplying a power to at least one of the plurality of loads, and a second communicating part for sending and receiving a signal to and from the second power supplying part; and

a controlling device for conducting each of a first operation control of the first power supplying part of the power supplying device and a second operation control of the second power supplying part of the power supplying device,

wherein the first communicating part and the second communicating part send and receive signals to and from each other, and the controlling device conducts the first operation control of the first power supplying part and the second operation control of the second power supplying part through the first communicating

part and the second communicating part.

15. The power supplying system as claimed in claim 14, wherein:

said first power supplying device includes a first interface part for conducting an interface with said controlling device; and

said controlling device includes a second interface part for conducting an interface with the first power supplying device,

wherein said controlling part conducts the first operation control of the first power supplying part through the first interface part and the second interface part.

16. The power supplying system as claimed in claim 15, wherein said controlling device is connected to the first communicating part through the first interface part and the second interface part and conducts the second operation control of the second power supplying part through the first communicating part and the second communicating part.

17. The power supplying system as claimed in claim 14, wherein said controlling device conducts the first operation control of the first power supplying part and the second operation control of the second power supplying part and conducts an operation

control of a function device including a predetermined function.

18. A serial communication apparatus for conducting a serial communication by a half-duplex communication between a first sending/receiving circuit and a second sending/receiving circuit in that at least one first sending/receiving circuit is connected to at least one second sending/receiving circuit through a transmission channel,

wherein each of said first sending/receiving circuit and said second sending/receiving circuit includes:

a sending circuit part for generating a serial data signal by superimposing a predetermined superimposing pulse over a send data signal having two values during a predetermined signal level, and outputting the serial data signal; and

a receiving circuit part for receiving the serial data signal sent from said sending circuit part, and extracting the send data signal by extracting the superimposing pulse from the serial data signal.

19. The serial communication apparatus as claimed in claim 18, wherein said sending circuit part superimposes a superimposing pulse, in which a reference pulse signal is inverted and which has a pulse width having a time T1, over the reference pulse signal starting from a predetermined start point and having a time T3 at a time point when a time T2 passes from the start

point, so that predetermined levels of the two values for one bit are shown in the send data signal and other levels of the two values for one bit are shown in the send data signal when the superimposing pulse is not superimposed at the time point when the time T2 passes from the start point, and

said sending circuit part further generates the serial data signal so that the time T1, the time T2, and the time T3 satisfy relationships of $T1 < T2 < T3$ and $(T1 + T2) < T3$, and outputs the send data signal successively every one bit.

20. The serial communication apparatus as claimed in claim 19, wherein said sending circuit part in the first sending/receiving circuit includes:

a T2 delaying circuit, to which a clock signal CLK synchronizing with the send data signal is input, for the clock signal CLK the clock signal CLK by delaying by the time T2;

a first T1 delaying circuit for outputting an output signal of the T2 delaying circuit by delaying by the time T1;

a first superimposing pulse generating circuit for generating the superimposing pulse having the pulse width having the time T1 from the output signal of the T2 delaying circuit and the output signal of the first T1 delaying circuit and outputting the superimposing pulse;

a T3 signal generating circuit for generating a signal having a pulse width having the time T3 from the clock signal CLK

and outputting the signal; and

a first output signal generating circuit for superimposing the superimposing pulse output from the first superimposing pulse generating circuit over the signal output from the T3 signal generating circuit in response to the send data signal, for generating the serial data signal being to send by sequentially generating a data signal for one bit, and for outputting the serial data signal to the transmission channel.

21. The serial communication apparatus as claim in claim 19, wherein said receiving circuit in said first sending/receiving circuit includes:

a first T1 eliminating circuit for eliminating the superimposing pulse from the serial data signal received from the transmission channel and outputting the serial data signal;

a first input signal delaying circuit for eliminating the superimposing pulse from the serial data signal received from the transmission channel, and for outputting the serial data signal by delaying by more than a time (T1 + T2),;

a first superimposing pulse extracting and outputting circuit for extracting the superimposing pulse from an output signal of the first T1 eliminating circuit, and an output signal of the first input signal delaying circuit; and

a first data extracting circuit for extracting and outputting the send data signal from an output signal of the first

superimposing pulse extracting circuit.

22. The serial communication apparatus as claimed in claim 19, wherein said receiving circuit part in said first sending/receiving circuit includes:

a first T1 eliminating circuit for eliminating and outputting the superimposing pulse from the serial data signal received from the transmission channel;

a first input signal delaying circuit for outputting an output signal of the first T1 eliminating circuit by delaying by more than a time (T1 + T2);

a first superimposing pulse extracting circuit for extracting and outputting the superimposing pulse from the serial data signal received from the transmission channel, the output signal of the first T1 eliminating circuit, the output signal of the first input signal delaying circuit; and

a first data extracting circuit for extracting and outputting the send data signal from an output signal of the first extracting circuit.

23. The serial communication apparatus as claimed in claim 21, wherein said first data extracting circuit generates a predetermined internal clock signal CLKi from the clock signal CLK, and outputs the send data signal subjected to be extracted, by synchronizing with the internal clock signal CLKi.

24. The serial communication apparatus as claimed in claim 19, wherein said receiving circuit part in said second sending/receiving circuit includes:

a second T1 eliminating circuit for eliminating and outputting the superimposing pulse from the serial data signal received from the transmission channel;

a second input signal delaying circuit for eliminating the superimposing pulse from the serial data signal received from the transmission channel, for outputting the serial data signal by delaying by more than a time (T1 + T2);

a second superimposing pulse extracting circuit for extracting and outputting the superimposing pulse from the serial data signal received from the transmission channel, an output signal of the second T1 eliminating circuit, and an output signal of the second input signal delaying circuit; and

a second data extracting circuit for extracting and outputting the send data signal from an output signal of the second superimposing pulse extracting circuit, and

said sending circuit in said second sending/receiving circuit includes:

a second T1 delaying circuit for outputting an output signal of said second input signal delaying circuit by delaying by a time T1;

a second superimposing pulse generating circuit for

generating and outputting the superimposing pulse having the pulse width having the time T1 from an output signal of the second T1 delaying circuit; and

a second output signal generating circuit for superimposing the superimposing pulse output from the second superimposing pulse generating circuit over the serial data signal received by said receiving circuit part in said second sending/receiving circuit in response to the send data signal, for generating the serial data signal to send, and for outputting the serial data signal to the transmission channel.

25. The serial communication apparatus as claimed in claim 19, wherein said receiving circuit part in said second sending/receiving circuit includes:

a second T1 eliminating circuit for eliminating and outputting the superimposing pulse from the serial data signal received from the transmission channel;

a second input signal delaying circuit for outputting an output signal of the second T1 eliminating circuit by more than a time (T1 + T2);

a second superimposing pulse extracting circuit for extracting and outputting the superimposing pulse from the serial data signal received from the transmission channel, an output signal of said second T1 eliminating circuit, and an output signal of said second input signal delaying circuit; and

a second data extracting circuit for extracting and outputting the send data signal from an output signal of said second superimposing pulse extracting circuit, and

said sending circuit part in said second sending/receiving circuit includes:

a second T1 delaying circuit for outputting an output signal of said second input signal delaying circuit by delaying by the time T1;

a second superimposing pulse generating circuit for generating and outputting the superimposing pulse having the pulse width having the time T1 from an output signal of the second T1 delaying circuit; and

a second output signal generating circuit for superimposing the superimposing pulse output from said second superimposing pulse generating circuit over the serial data signal received by said receiving circuit part in said second sending/receiving circuit, for generating the serial data signal to send, and for outputting the serial data signal to the transmission channel.

26. The serial communication apparatus as claimed in claim 24, wherein said second output signal generating circuit superimposes the superimposing pulse output from said second superimposing pulse generating circuit over the serial data signal received by said receiving circuit part and outputs the serial

data signal to the transmission channel when the serial data signal received by said receiving circuit in said second sending/receiving circuit is a predetermined signal level.

27. The serial communication apparatus as claimed in claim 19, wherein said second sending/receiving circuit uses the serial data signal in which data is not included and which is sent from said first sending/receiving circuit, as the reference pulse signal in a case of sending the data signal to said first sending/receiving circuit.

28. The serial communication apparatus as claimed in claim 27, wherein:

said first sending/receiving circuit generates the serial data signal by superimposing the superimposing pulse over the send data signal input from a predetermined host device during a predetermined signal level, and outputs the serial data signal to said second sending/receiving circuit through the transmission channel; and

said second sending/receiving circuit extracts the send data signal by extracting the superimposing pulse from the serial data signal input from the transmission channel, and outputs the send data signal being extracted to a predetermined slave device.

29. The serial communication apparatus as claimed in claim 28, wherein:

said second sending/receiving circuit generates the serial data signal by superimposing the superimposing pulse over the send data signal input from the slave device during a predetermined signal level, and outputs the serial data signal to said first sending/receiving circuit through the transmission channel; and

said first sending/receiving circuit extracts the send data signal by extracting the superimposing pulse from the serial data signal input from the transmission channel, and outputs the send data signal being extracted to the host device.